a fourth external terminal for receiving a designating signal designating one of said operational modes;

first means, coupled to said first, second and third external terminals, for detecting levels of said row address strobe signal, said column address strobe signal and said write enable signal; and

second means, coupled to said first means and to said fourth external terminal, for setting said designating signal into a holding circuit in response to said column address strobe signal being at a logic "low" level, said write enable signal being at a logic "low" level and said row address strobe signal being at a logic "low" level.

19. 4 An address multiplex dynamic RAM according to claim ~~18~~, 5 wherein said fourth external terminal is used for receiving an address signal in a first period of time and for receiving said designating signal in a second period of time.

20. 7 An address multiplex dynamic RAM according to claim ~~19~~; 6 wherein input data is written into at least one of said memory cells on the basis of a designated one of said operational modes.

21. 8 An address multiplex dynamic RAM according to claim ~~20~~, 7 wherein said at least one of said memory cells is designated on the basis of said address signal supplied to said fourth external terminal in said first period of time.

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22. In an address multiplex dynamic RAM having a plurality of memory cells and a plurality of operational modes, a circuit arrangement comprising:

a first external terminal for receiving a row address strobe signal;

a second external terminal for receiving a column address strobe signal;

a third external terminal for receiving a write enable signal;

a fourth external terminal for receiving a designating signal designating one of said operational modes;

a first circuit, coupled to said first, second and third external terminals, detecting levels of said row address strobe signal, said column address strobe signal and said write enable signal; and

a second circuit, coupled to said first means and to said fourth external terminal, for setting said designating signal into a holding circuit in response to said column address strobe signal being at a logic "low" level, said write enable signal being at a logic "low" level and said row address strobe signal being at a logic "low" level.

23. An address multiple dynamic RAM according to claim 22, wherein said fourth external terminal is used for receiving an address signal in a first period of time and for receiving said designating signal in a second period of time.

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~~24.~~ 9 In an address multiplex dynamic RAM having a plurality of memory cells and a plurality of operational modes, a circuit arrangement comprising:

a first external terminal for receiving a row address strobe signal;

a second external terminal for receiving a column address strobe signal;

a third external terminal for receiving a write enable signal;

a plurality of fourth external terminals for receiving designating signals designating one ~~or~~ of said operational modes;

a first circuit, coupled to said first, second and third external terminals detecting levels of said row address strobe signal, said column address strobe signal and said write enable signal; and

a second circuit, coupled to said first circuit and to said plurality of fourth external terminals, setting said designating signals into a holding circuit in response to said column address strobe signal being at a logic "low" level, said write enable signal being at a logic "low" level and said row address strobe signal being at a logic "low" level.

~~25.~~ 10 An address multiplex dynamic RAM according to claim ~~24~~, 9 wherein said plurality of fourth external terminals are used for receiving address signals in a first period of time and for receiving said designating signals in a second period of time.

26. 11 An address multiple dynamic RAM according to claim 25, 10 wherein input data is written into at least one of said memory cells on the basis of a designated one of said operational modes.

27. 12 An address multiplex dynamic RAM according to claim 26, 11 wherein said at least one of said memory cells is designated on the basis of said address signals supplied to said plurality of fourth external terminals.

28. 13 An address multiplex dynamic RAM according to claim 25, 10 further comprising a fifth external terminal for receiving a write signal, wherein said write signal is written into said at least one of said memory cells in said operational mode defined by said designating signal set in said holding circuit. --

REMARKS

Entry of this Amendment prior to examination is respectfully requested.

By the present Amendment, new claims 18-28 are submitted for examination together with claims 14-17 (which were allowed in the parent application). New claims 18-28 are similar to the allowed claims 14-17 from the parent application, but emphasize a slightly different aspect of the present invention. For example, claim 14 defines that the second means sets one of the operational modes in response to a designating signal as well as in response to the column

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